TSMC-03-405

February 27, 2004

Commissioner for Patents P.O.Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Req. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/738,416 12/17/03

Chia-Chen Liu et al.

METHOD OF FORMING A FLOATING GATE FOR A SPLIT-GATE FLASH MEMORY DEVICE

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March / , 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

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U.S. Patent 6,570,790 to Harari, "Highly Compact EPROM and Flash EEPROM Devices," describes several EPROM and flash EEPROM devices showing alternative floating gate shapes.

U.S. Patent 6,531,734 to Wu, "Self-aligned Split-gate
Flash Memory Cell having an Integrated Source-side Erase
Structure and its Contactless Flash Memory Arrays," discloses a split-gate flash memory device and method of manufacture.

U.S. Patent 6,171,906 to Hsieh et al., "Method of Forming Sharp Beak of Poly to Improve Erase Speed in Split Gate Flash," discloses a split-gate flash device and method of manufacture showing a floating gate with an erasing tip formed using LOCOS.

U.S. Patent 6,165,845 to Hsieh et al., "Method to Fabricate Poly Tip in Split-gate Flash," describes a split-gate flash device and method of manufacture.

Sincerely,

Stephen B. Ackerman,

Reg. No. 37761

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